

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A satellite communication system comprising:
 - a satellite earth station operably coupled to at least one data network; and
 - a plurality of satellite modems, each satellite modem of the plurality of satellite modems communicating in an upstream and downstream data communication mode with the satellite earth station via at least one servicing satellite,wherein the satellite earth station includes:
 - a host processor for receiving data packets from the at least one data network and processing ~~[[the]]~~ Data Over Cable Service Interface Specification (DOCSIS) management packets,
 - a DOCSIS Media Access Control (MAC) coupled to the host processor for encrypting ~~[[the]]~~ a transmit packet data from ~~[[the]]~~ a host memory, framing data in MAC headers and inserting MAC timestamps in the transmit packet data,
 - a satellite modulator coupled to the DOCSIS MAC for modulating ~~[[the]]~~ an encrypted transmit packet data to generate downstream output data for transmission to at least one of the plurality of satellite modems, and
 - a turbo decoder coupled to the burst demodulator and the DOCSIS MAC for decoding ~~[[the]]~~ demodulated data from the burst demodulator and sending ~~[[the]]~~ decoded data to the DOCSIS MAC, wherein the DOCSIS MAC sends DOCSIS management packets portion of the decoded data to the host processor

and sends transmit packet data portion of the decoded data to the at least one data network.

2. (Original) The satellite communication system of claim 1, wherein the data network is the Ethernet.

3. (Original) The satellite communication system of claim 1 further comprising an RS Decoder for correcting errors of the decoded signal from the turbo decoder.

4. (Original) The satellite communication system of claim 1, wherein the DOCSIS MAC comprises:

a SPI controller for supporting a downstream channel and at least one upstream channel;

an encryption engine for encrypting the downstream data;

a decryption engine for decrypting the upstream data;

a formatter for formatting downstream data into Motion Picture Expert Group (MPEG) frames; and

a timing generator for inserting DOCSIS time stamps at programmable intervals.

5. (Original) The satellite communication system of claim 1, wherein the burst demodulator comprises:

an analog front end (AFE) circuit for accepting an analog input signal and generating a digital signal;

a digital filter coupled to the AFE circuit for filtering the digital signal;
a quadrature amplitude (QAM) demodulator coupled to the digital filter for word detection of programmable length and pattern in a burst preamble of the digital signal;
an adaptive equalizer coupled to the QAM demodulator for characterizing a RF channel response; and
a forward error correction (FEC) decoder coupled to the adaptive equalizer for decoding of FEC code.

6. (Original) The satellite communication system of claim 1, wherein the FEC decoder comprises a programmable de-scrambler; a programmable reed-Solomon (RS) decoder; a byte deinterleaver; and FEC interface circuit.

7. (Original) The satellite communication system of claim 5, wherein the adaptive equalizer includes an Ingress cancellation circuit for canceling ingress noise and removing inter-symbol interference.

8. (Original) The satellite communication system of claim 5, further comprising a microcontroller for programming of the burst demodulator.

9. (Original) The satellite communication system of claim 5, further comprising a channel B input interface configured to accept a direct RF analog input.

10. (Original) The satellite communication system of claim 1, wherein the turbo decoder comprises:

dual analog-to-digital converters (ADCs) for sampling a baseband IQ analog waveform;

a phase/frequency recovery circuit coupled to the dual ADCs for recovering the phase and frequency of the sampled waveform;

a variable demodulator for demodulating the recovered signal;

a forward error correction (FEC) decoder coupled to the demodulator for FEC decoding of the modulated signal; and

a turbo decoding circuit coupled to the demodulator for turbo decoding of the modulated signal.

11. (Original) The satellite communication system of claim 10, wherein the turbo decoding circuit comprises: a Viterbi decoder, a synchronization and deinterleaver, and a reed-Solomon (RS) decoder.

12. (Original) The satellite communication system of claim 10, further comprising a microcontroller for system configuration, control, and monitoring functions.

13. (Original) The satellite communication system of claim 10, further comprising a downstream circuit coupled to the DOCSIS MAC for reformatting the data into a byte-wide stream and forward the bytes to the satellite modulator.

14. (Original) A method for a satellite communication in compliance with a Data Over Cable Service Interface Specification (DOCSIS) standard, the method comprising:

- receiving a radio frequency (RF) upstream signal;
- demodulating the received RF signal to generate soft decision quadrature-phase-shift keying (QPSK) output signal;
- turbo decoding the QPSK output signal;
- decoding the turbo decoded output signal by a Reed-Solomon (RS) decoder;
- assembling DOCSIS packets to the RS decoded signal; and
- forwarding the assembled data to a data network.

15. (Original) The method of claim 14, further comprising:

- receiving DOCSIS-compliant data encoded with a Reed-Solomon encoding scheme from the data network;
- turbo-encoding the DOCSIS-compliant data;
- generating baseband-frequency in-phase and quadrature-phase components of the turbo-encoded DOCSIS-compliant data;
- converting the turbo-encoded DOCSIS-compliant data to one or more analog signals for downstream satellite data transmission.

16. (Original) The method of claim 15, further comprising interpolating the baseband-frequency in-phase and quadrature-phase components to a common sample rate that is higher than a plurality of DOCSIS-compliant bandwidth sample rates.

17. (Original) The method of claim 16, further comprising digitally pre-compensating the common sample rate baseband-frequency in-phase and quadrature-phase components for impairments encountered in one or more subsequent processes;

converting digitally pre-compensated common sample rate baseband-frequency in-phase and quadrature-phase components to one or more analog signals; and

18. (Currently Amended) A satellite earth station system for upstream and downstream data communication comprising:

a host computer coupled to a data network for receiving data packets from a data network and processing [[the]] Data Over Cable Service Interface Specification (DOCSIS) management packets;

a demodulator/Media Access Control (MAC) card coupled to the host processor including:

a DOCSIS MAC coupled to the host computer for encrypting transmit packet data from the data network responsive to [[the]] processed DOCSIS management packets from the host computer,

a burst demodulator for demodulating upstream data received from a satellite modem, and

a turbo decoder coupled to the burst demodulator and the DOCSIS MAC for decoding the demodulated data from the burst demodulator and sending the decoded data to the DOCSIS MAC, wherein the DOCSIS MAC sends DOCSIS

management packets portion of the decoded data to the host computer and sends transmit packet data portion of the decoded data to the data network; and a satellite modulator coupled to the demodulator/MAC card for modulating the encrypted transmit packet data from the DOCSIS MAC to generate downstream output data for transmission to the satellite modem.

19. (Original) The satellite earth station system of claim 18, wherein the demodulator/MAC card is embodied in a pluggable circuit board card resident in a PCI chassis and the host computer is a personal computer (PC).

20. (Original) The satellite earth station system of claim 18, wherein the data network is the Ethernet.

21. (Original) The satellite earth station system of claim 19, wherein the DOCSIS MAC and the PC communicate via a PCI bus.